In the Specification

Please replace the paragraph beginning on page 10, line 11 through page 11, line 4 with the following amended paragraph:

In operation of the emulator 13, it may carry out various watches on events occurring within the processor. This is illustrated in Figure 5 in which the emulator 13 is shown as carrying out a program count watch 100 on instructions fetched from the program memory and supplied to the control unit 32. It may also watch data accesses (load or store) between the core and the data memory via the data memory controller. This is shown in Figure 5 as a data/register watch [[81]] 101 which may watch addresses used for data memory accesses in the local data memory or errors in a system memory ~~as shown in Figure 8~~. The data/register watch of Figure 5 is carried out by a data memory hook [[81]] 80 as shown in Figure 2. Indications of the program count which has been watched are supplied by the control unit 32 on line 103 to a synchronisation unit 104. A commit signal of zero or one is generated by the data unit 33 when the guard value has been resolved by the data unit thereby indicating whether the instruction is executed or not. The commit signal is provided on line 106 to the synchronisation unit 104. Line 106 corresponds to line 97 of Figure 4. Similarly when a load or store operation is executed by the address unit 34 a signal is provided on line 107 to the synchronisation unit 104 to indicate if a load or store is sent or not sent to the memory controller 37. A watch hit on particular addresses and/or data values is provided on line 108 to the synchronisation unit 104. The synchronisation unit comprises a plurality of FIFO's which will be described with reference to Figure 6. The output of the synchronisation unit 104 is fed to a trigger unit 110 when the result of synchronisation requires a trigger operation by the emulator 13. It also supplies an output to a trace unit 111 in order to establish a required trace in the emulator 13.